CLAIMS:-

1. Apparatus for depacketizing and aligning packetized input data, having:

an input memory for receiving storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating a payload size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

an input buffer for receiving said data words from the word formatter and storing these, and for transferring the data words to the data processing means, to effect said separate receiving of said payload;

said data processing means for effecting said data processing using the received said data words.

2. Apparatus as claimed in claim 1 having a data input interface through which the input data is transferred to the input memory, said data input interface for performing hand shaking with a packetized data source of said input data.

3. Apparatus as claimed in claim 1 or claim 2 wherein the input memory has a fullness level detector for generating a level filled signal when the input data received thereby is such as to fill the input memory to a predetermined level, and said data processing means is responsive to generation of said level filled signal to execute said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating said payload size signal.

4. Apparatus as claimed in claim 3 having an interrupt controller, for receiving said level filled signal and generating an interrupt signal pursuant to receipt thereof, said data processing means being arranged for receipt of said interrupt signal and, on receipt thereof, for executing said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal.

5. Apparatus as claimed in claim 3 or claim 4, as appended directly or indirectly to claim 2, wherein the input memory has a further fullness level detector for generating and directing to said data input interface a further level filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, said data input interface being responsive to receipt of said further level filled signal to generate a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source.

6. Apparatus as claimed in any preceding claim wherein the input memory is controlled whereby said input data comprising said packet is removed from the input memory and relaced by fresh input data, pursuant to the transfer to the data processing means of said words representing the data packet to the data the apparatus being arranged for repetitive depacketizing and aligning of data packets and data processing thereof, the data processing means being arranged for repetitively and alternatingly executing a step comprising said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal, and a step comprising said separately receiving and effecting data processing of the payload of the data packet.

7. Apparatus as claimed in any preceding claim wherein the data processing means includes a digital signal processor, data/program memory, DMA controller and input buffer, each in data communication via a bus.

8. Apparatus as claimed in claim 7, wherein the word formatter is arranged for generating a DMA request signal when a said data word is formed thereby, and the DMA controller is responsive to said DMA request signal to generate and direct a transfer signal to the digital signal

processor, the digital signal processor being responsive to the transfer signal to enable the DMA controller to move the data word from the word formatter to the input buffer for subsequent processing.

9. Apparatus as claimed in claim 5 wherein said input memory is a first in first out memory.

10. Apparatus as claimed in any preceding claim wherein the data processing means is arranged to execute said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

11. Apparatus as claimed in any preceding claim wherein the data processing means, pursuant to said detecting and identifying the data packet, extracts timing information from the input data.

12. Apparatus as claimed in any preceding claim wherein the data processing means, pursuant to said detecting and identifying the data packet, extracts side information from the input data.

13. A method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input data outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means; and

effecting data processing on the data packet represented by the data words transferred thereto, using the transferred data words.

14. A method as claimed in claim 13 wherein the input data is transferred to the input memory via an data input interface which performs hand shaking with a packetized data source of said input data.

15. A method as claimed in claim 13 or claim 14 including the step of generating a level filled signal when the input data received by the input memory is such as to fill the input memory to a predetermined level, and causing said data processing means to effect said detecting, identifying and determining payload size of the data packet, and to said generate payload size signal, pursuant to generation of the level filled signal.

16.(Amended) A method as claimed in claim 15 including the step of generating an interrupt signal from said level filled signal and directing said interrupt signal to said data processing means to cause said data processing means to effect said receiving and outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and to generate said payload size signal.

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17. A method as claimed in claim 15 or claim 16, as appended directly or indirectly to claim 14, including the step of generating and directing to said data input interface a further level filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, and causing said data input interface to generate, responsive to receipt thereby of said further level filled signal, a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source.

18. A method as claimed in any one of claims 13 to 17 wherein the input memory is controlled whereby said input data comprising a said packet is removed from the input memory and replaced by fresh input data pursuant to the transfer of said words representing that data packet to the data processor, and wherein a step comprising said receiving and outputted input

data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal indicative of the size of the payload, and a step comprising effecting data processing of the payload are repetitively and alternatingly executed.

19. A method as claimed in claim 18, including generating a DMA request signal when a said word is formed, and applying the DMA request signal to a digital signal processor forming part of said data processing means to cause the digital signal processor to enable a DMA controller to move that data word from the word formatter to an input buffer of the data processor for subsequent processing.

20. A method as claimed in any one of claims 13 to 19 wherein said input memory is a first in first out memory.

21. A method as claimed in any one of claims 13 to 20 wherein the data processing means executes said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

22. A method as claimed in any one of claims 13 to 21 wherein the data processing means extracts timing information from the input data pursuant to said detecting and identifying the data packet.

23. A method as claimed in any one of claims 13 to 22 wherein the data processing means extracts side information from the input data pursuant to said detecting and identifying the data packet.

24. Apparatus for depacketizing and aligning packetized input data, having:

an input memory for receiving storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating a payload

size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

means for transferring the data words to the data processing means, to effect said separate receiving of said payload.

25. A method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal whereby to cause payload units which form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing the in said input buffer;

transferring said data words to the data processing means.

26. (Deleted)

27. (Deleted)

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28. (Deleted)

29. (Deleted)

AMENDED SHEET